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Charissa D. Wheeler

## APPLICATION FOR UNITED STATES LETTERS PATENT

# SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Kyung Yun Jung, a citizen of Republic of Korea, residing at 205-703, Hyunjin Evervil, Sinhae-Ri, Kanam-Myoun, Yeosu-Gun, Kyunggi-Do, 469-885 have invented a new and useful **A SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**, of which the following is a specification.

A SEMICONDUCTOR DEVICE AND METHOD OF  
MANUFACTURING THE SAME

RELATED APPLICATION

[0001] This application is related to Korean Patent Application No. 10-2002-0087274 filed on December 30, 2002, which is incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates generally to semiconductor devices and, more particularly, to a semiconductor device having a variable capacitance capacitor and a method of manufacturing the same

BACKGROUND

[0003] Generally, a capacitor constitutes a unit cell of a semiconductor device together with a metal oxide semiconductor (MOS) transistor, providing a function of frequency modulation. As shown in Figure 1, such a capacitor generally has a structure in which a bottom electrode 12, a dielectric layer 14, and an upper electrode 15 are successively formed on a semiconductor substrate 11. Recently, with a refinement of a design rule for semiconductor devices, the area occupied by the capacitor in the semiconductor device is reduced to enable the fabrication of a capacitor with a large capacitance in a reduced area. However, the conventional capacitor shown in Figure 1 has a structure in which the bottom electrode 12 is formed in a planar shape, which limits the maximum capacitance that may be employed in a micro or semiconductor device.

**[0004]** To satisfy the need for a capacitor with large capacitance, at least one study has concentrated on development of a capacitor having increased capacitance in a unit area. As a result, as shown in Figure 2, a method of maximizing a capacitance of capacitor in which a bottom electrode 22 has been formed as an uneven shape to increase an effective area contacting with a dielectric layer 23 has been proposed. In addition, a method of maximizing a capacitance by use of various capacitor structures has also been provided. However, because the conventional capacitor has a fixed capacitance, regardless of its capacitance level, it has a problem in adapting to a presently used semiconductor device having a multi-function.

#### BRIEF DESCRIPTION OF THE DRAWINGS

- [0005]** Figure 1 is a cross-sectional view of a known capacitor structure.
- [0006]** Figure 2 is a cross-sectional view of another known capacitor structure.
- [0007]** Figure 3 is a perspective view of an example semiconductor device.
- [0008]** Figure 4 is a cross-sectional view taken along a line of A-A' of Figure 3.
- [0009]** Figures 5A to 5D are cross-sectional views depicting an example method of manufacturing a semiconductor device.
- [0010]** Figure 6 is a circuit diagram depicting one manner in which the semiconductor device of Figure 3 may be used.

#### DETAILED DESCRIPTION

**[0011]** As described in greater detail below, an example semiconductor device includes a capacitor having a bottom electrode, a dielectric layer and an upper electrode, formed on a semiconductor substrate. The example semiconductor device also includes a first insulating layer formed on the semiconductor substrate to cover the capacitor, a first contact plug formed in a first via hole of the first insulating layer

and electrically connected to the bottom and upper electrodes, a first metal wiring formed on the first insulating layer and electrically connected to the bottom electrode through the first contact plug, and a second contact plug formed on the first insulating layer and electrically connected to the upper electrode through the first contact plug. Still further, the example semiconductor device includes a second insulating layer formed on the first insulating layer to cover the first metal wiring and the second contact plug, an anti-fuse formed in a certain thickness in a second via hole of the second insulating layer and electrically connected to the second contact plug, a third contact plug filling the second via hole on the anti-fuse, and a second metal wiring formed on the second insulating layer and electrically connected to the third contact plug. Preferably, the first and second metal wirings are perpendicular to each other.

**[0012]** A example method of manufacturing the example semiconductor device includes forming a capacitor having a bottom electrode, a dielectric layer and an upper electrode on a semiconductor substrate; forming a first insulating layer on the semiconductor substrate to cover the capacitor; forming a plurality of first via holes exposing the surfaces of the bottom and upper electrodes by selectively patterning the first insulating layer; forming a plurality of first contact plugs by filling the via holes with metal materials; forming a first metal wiring connected to the bottom electrode through the first contact plug and a second contact plug connected to the upper electrode through the first contact plug on the first insulating layer; forming a second insulating layer on the first insulating layer to cover the first metal wiring and the second contact plug; forming a plurality of second via holes exposing the surface of the second contact plug by selectively patterning the second insulating layer; successively depositing the first and second metal layers on the second insulating layer including the second via hole; forming an anti-fuse and a third contact plug in

the second via hole by planarizing the first and second metal layers with the second insulating layer; and forming a second metal wiring electrically connected to the anti-fuse and the third contact plug.

**[0013]** Using the example methods and apparatus described herein, the capacitance of a capacitor may be varied via a program, for example.

**[0014]** Figure 3 is a perspective view of an example semiconductor device and figure 4 is a cross-sectional view taken along a line of A-A' of Figure 3. As shown in Figures 3 and 4, an example semiconductor device includes a capacitor having a bottom electrode, a dielectric layer and an upper electrode, successively formed on a semiconductor substrate. A first insulating layer 102 is formed on the semiconductor substrate to cover the upper electrode 100c. A plurality of via holes exposing the bottom and upper electrodes are formed on a certain portion of the first insulating layer and first contact plugs 104a are formed by filling the plurality of via holes with metal material.

**[0015]** A first metal wiring electrically connected to the bottom electrode 100a through the first contact plug 104a is formed on one side of the first insulating layer 102 and a plurality of second contact plugs 108a electrically connected to the upper electrode 100c through the first contact plug 104a are formed on the other side of the first insulating layer 102.

**[0016]** A second insulating layer 106 is formed on the semiconductor substrate to cover the first metal wiring 104 and the second contact plug 108a. A plurality of via holes exposing the second contact plugs 108a are formed on a certain portion of the second insulating layer 106 and anti-fuse 108c is formed in a certain thickness in each via hole. A third contact plug 108b is formed on the anti-fuse, which serves to vary the capacitance. A second metal wiring 108 electrically connected to the third contact

plug 108b is formed on the second insulating layer covering the third contact plug 108b.

**[0017]** Figures 5A to 5D are cross-sectional views depicting an example method of manufacturing the example semiconductor device described herein.

**[0018]** First, as shown in Figure 5A, using a conventional capacitor formation process, a capacitor 100 having a bottom electrode 100a, a dielectric layer 100b and an upper electrode 100c is formed on a semiconductor substrate (not shown). The upper and bottom electrodes 100c and 100a may be formed of a poly silicon layer or a metal layer.

**[0019]** Then, a first insulating layer 102 is formed on the semiconductor substrate including the upper electrode 100c. Successively, a photoresist (not shown) is coated on the first insulating layer 102, and the first insulating layer 102 is selectively etched and removed by a conventional photolithography process and an etching process. As a result, a first via hole 103 exposing the surfaces of the bottom and upper electrodes, is formed by the selective etching of the first insulating layer 102.

**[0020]** In such state, as shown in Figure 5B, a metal layer such as tungsten layer is deposited on the first insulating layer 102 to sufficiently fill the first via hole 103. Then, using a chemical mechanical polishing (CMP) process, the tungsten layer is planarized with the first insulating layer 102, so that a first contact plug 104a that fills the first via hole with the metal layer is formed.

**[0021]** Then, as shown in Figure 5C, a metal layer for forming a first metal wiring is deposited on the first insulating layer 102 and on the first contact plug 104a, by using such as a sputtering process. Then, the metal layer for the first metal wiring is selectively patterned by a photolithography and an etching process, thus forming a

first metal wiring 108a and a second contact plug 104 electrically connected to the first contact plug 104a.

**[0022]** Then, a second insulating layer 106 is deposited on the first insulating layer to cover the first metal wiring 104 and the second contact plug 108a. Then, a photoresist (not shown) is coated on the second insulating layer, and the second insulating layer 106 is selectively etched and removed by a conventional photolithography process and an etching process, thus forming a second via hole 107. A surface of the second contact plug 108a is exposed by the second via hole 107.

**[0023]** In a state that the second via hole 107 has been formed, as shown in Figure 5D, a metal layer, i.e., a first metal layer for forming an anti-fuse is formed in a certain thickness on the semiconductor substrate including in the second via hole 107. Then, a conductive metal layer, i.e., a second metal layer is formed on the semiconductor substrate including the first metal layer to sufficiently fill the second via hole. Then, the first metal layer and second metal layer are planarized with the second insulating layer 106. Thus, the anti-fuse 108c is formed in the second via hole 107 and a third contact plug 108b is formed inside the anti-fuse.

**[0024]** Figure 6 is an example circuit diagram for illustrating the operation of the semiconductor device of Figure 3. The construction of the circuit diagram of Figure 6 is similar or identical to that of Figure 3.

**[0025]** First, a specific capacitance of the capacitor is predetermined. For example, an example in which the capacitance is equal to  $C1+C2+C3$  is described below.

**[0026]** Because a program is not operating, transistors TR1, TR2, TR3 and TR4 are in an off state by signal S1 and a stored capacitance between A1 and A2 is equal

to zero. Herein, T1, T2, T3 and T4 are input signals for selecting one capacitor and for programming an anti-fuse switch.

[0027] A programmable (e.g., controlled by a program) voltage is applied between T1 and T3 to turn the anti-fuse connected to C1 on. Then, TR1, TR2, TR3 and TR4 are turned on by S1. Herein, the stored capacitance between A1 and A2 is equal to C1. Then, programmable voltage is applied between T1 and T4 so as to connect C2. Then, TR1, TR2, TR3 and TR4 are turned on by S1. Herein, the stored capacitance between A1 and A2 is equal to C1+C2. Successively, programmable voltage is applied between T2 and T3 to connect C3. Then, TR1, TR2, TR3 and TR4 are turned on by S1. Herein, the stored capacitance between A1 and A2 is equal to C1+C2+C3. In this manner, the capacitance may be varied (e.g., by a user) as desired via a program or the like.

[0028] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.